

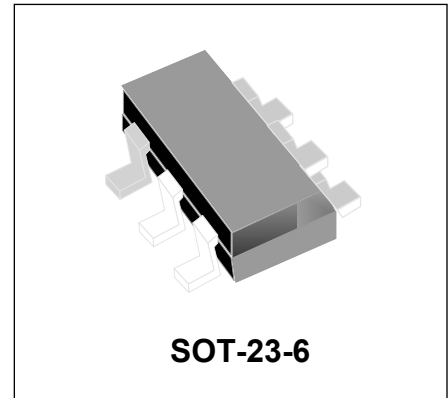


Features

- Solid-state silicon-avalanche technology
- 250 Watts Peak Pulse Power per Line ($t_p=8/20\mu s$)
- Low operating and clamping voltages
- Protects five I/O lines
- Working Voltage: 5 V
- Low Leakage

IEC Compatibility (EN61000-4)

- IEC 61000-4-2 (ESD) $\pm 30kV$ (air), $\pm 30kV$ (contact)
- IEC 61000-4-4 (EFT) 40A (5/50ns)
- IEC 61000-4-5 (Lightning) 14A (8/20 μs)



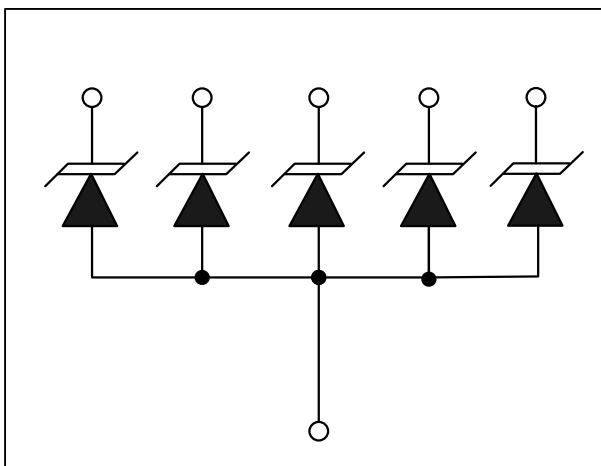
Mechanical Characteristics

- SOT-23-6 package
- Molding compound flammability rating: UL 94V-0
- Marking: Marking Code
- Packaging: Tape and Reel
- RoHS Compliant

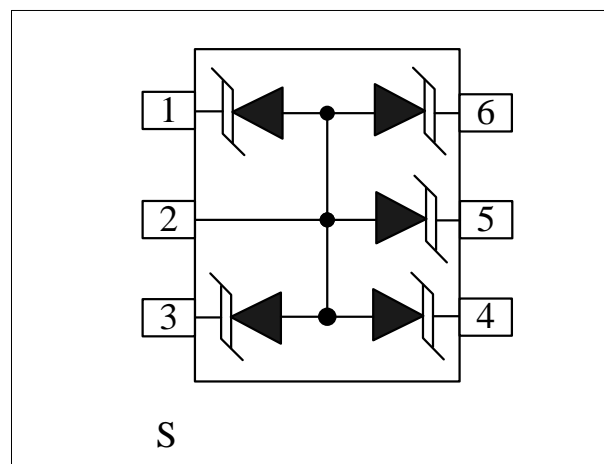
Applications

- Cell phone Handsets & Accessories
- Personal Digital Assistants (PDAs)
- Notebook, Laptop, and Palmtop Computers
- Portable Instrumentation
- Digital Cameras
- MP3 Player

Circuit Diagram



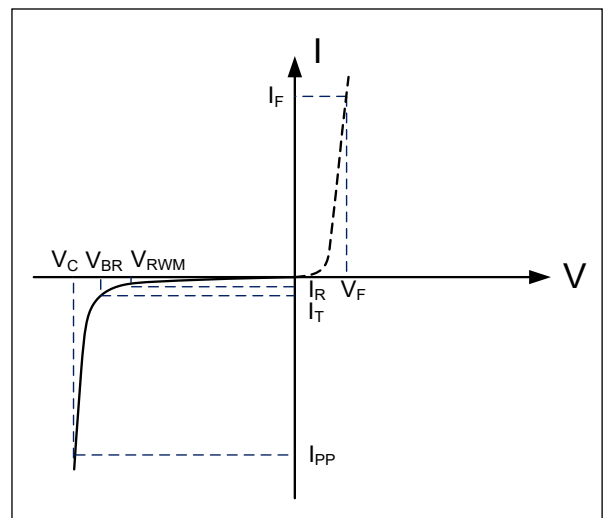
Schematic & PIN Configuration



Absolute Maximum Rating			
Rating	Symbol	Value	Units
Peak Pulse Power ($t_p = 8/20\mu s$)	P_{PP}	250	Watts
Peak Forward Voltage ($I_F = 1A, t_p = 8/20\mu s$)	V_{FP}	1.5	V
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Parameters (T=25°C)

Symbol	Parameter
I_{PP}	Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Reverse Stand-Off Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F



Electrical Characteristics

DW05MSC-S						
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				5.0	V
Reverse Breakdown Voltage	V_{BR}	$I_T = 1mA$	6.0			V
Reverse Leakage Current	I_R	$V_{RWM} = 5V, T = 25^\circ C$			0.5	μA
Peak Pulse Current	I_{PP}	$t_p = 8/20\mu s$			14	A
Clamping Voltage	V_C	$I_{PP} = 1A, t_p = 8/20\mu s$			9.5	V
Clamping Voltage	V_C	$I_{PP} = 14A, t_p = 8/20\mu s$		15	17	V
Junction Capacitance	C_j	Between I/O pins and Ground $V_R = 0V, f = 1MHz$		90	100	pF

Typical Characteristics

Figure 1: Peak Pulse Power vs. Pulse Time

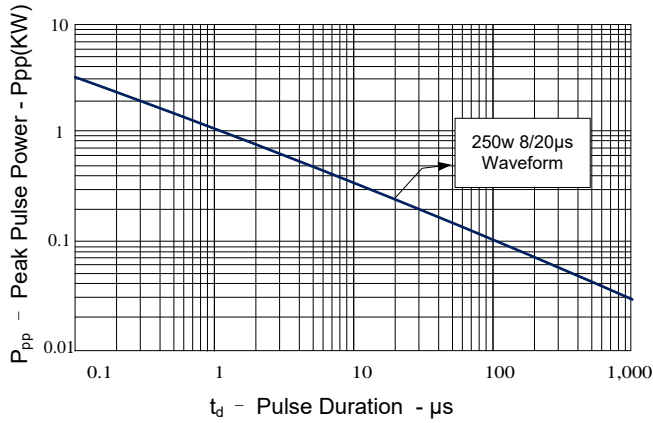


Figure 2: Power Derating Curve

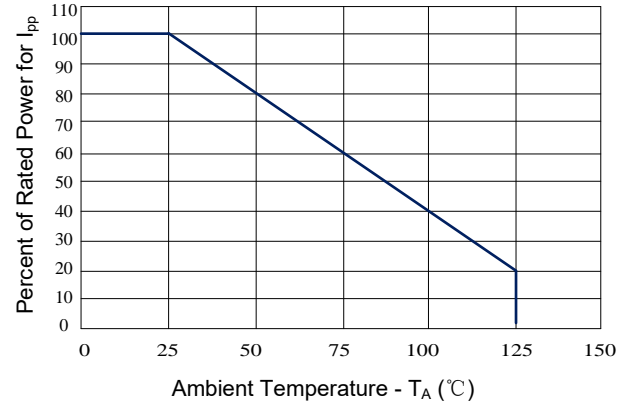


Figure 3: Clamping Voltage vs. Peak Pulse Current

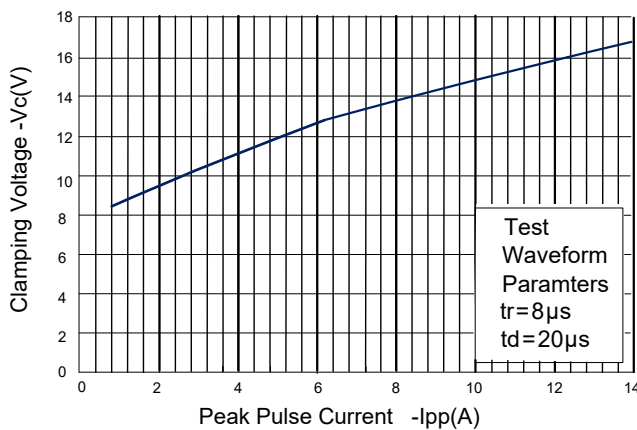


Figure 4: Normalized Junction Capacitance vs. Reverse Voltage

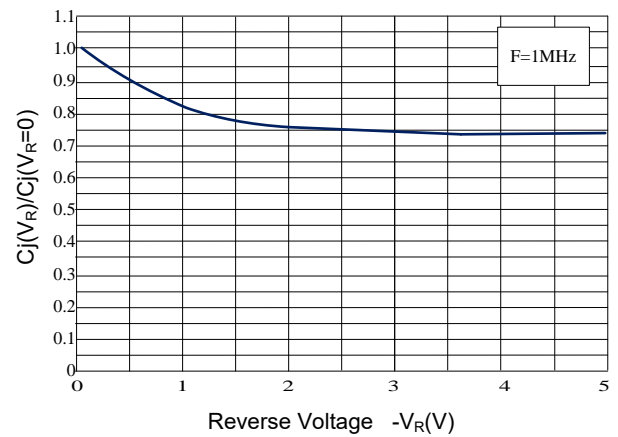


Figure 5: Pulse Waveform

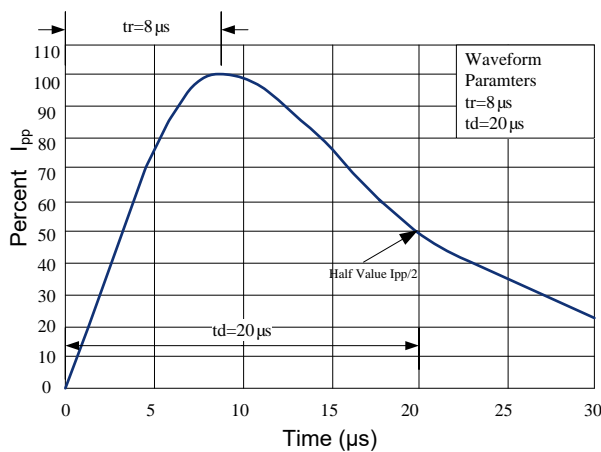
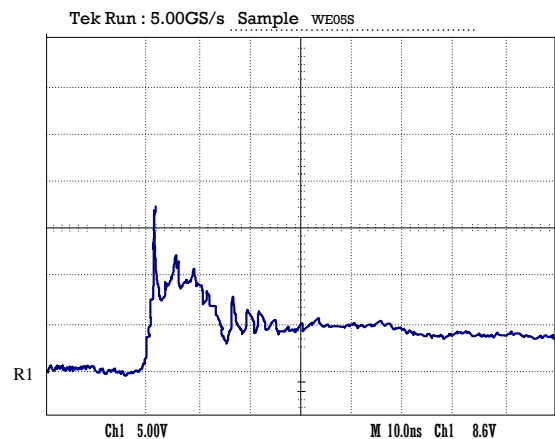


Figure 6: ESD Clamping(8kV Contact per IEC 61000-4-2)



Application Information

The DW05MSC-S Series are TVS arrays designed to protect I/O or data lines from the damaging effects of ESD or EFT. This product provides unidirectional protection; the device is connected as follows:

UNIDIRECTIONAL COMMON-MODE CONFIGURATION

The DW05MSC-S Series provides up to five(5) lines of protection in a common-mode configuration as depicted in Figure 7. Circuit connectivity is as follows:

- I/O 1 is connected to Pin 6.
- I/O 2 is connected to Pin 5.
- I/O 3 is connected to Pin 4.
- I/O 4 is connected to Pin 3.
- I/O 5 is connected to Pin 1.
- Pin 2 is connected to ground.

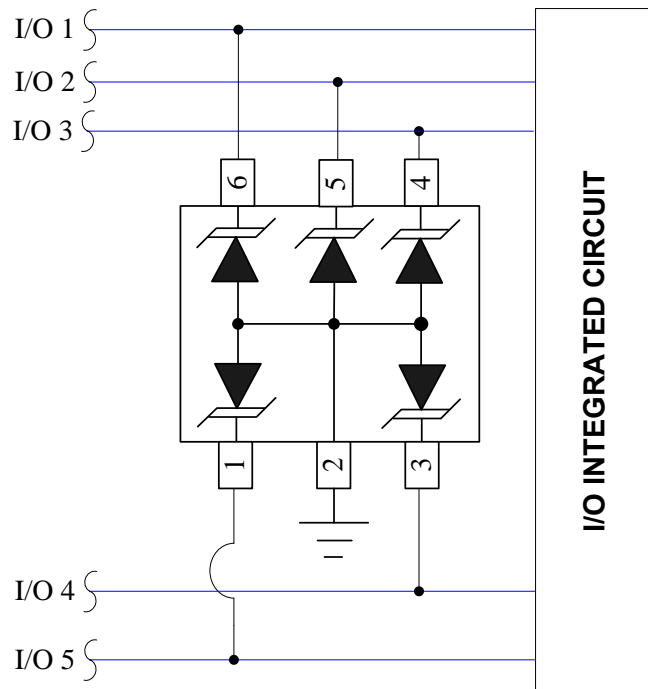


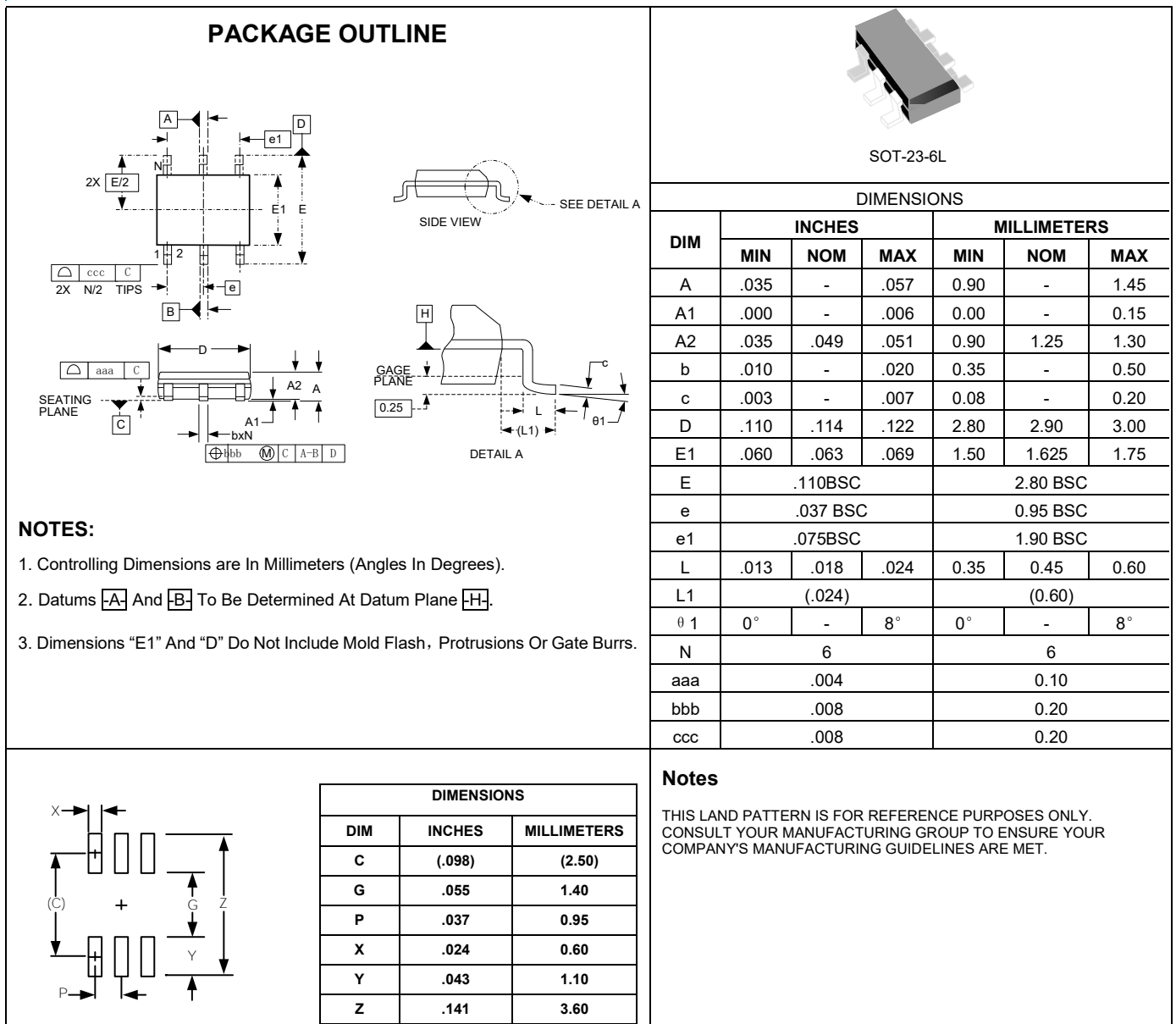
Figure 7 Unidirectional Configuration Common-Mode I/O Port Protections

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

- The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.
- The path length between the TVS device and the protected line should be minimized.
- All conductive loops including power and ground loops should be minimized.
- The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.
- Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

Outline Drawing – SOT-23-6L



Marking Codes

Part Number	DW05MSC-S
Marking Code	05S

Package Information

Qty: 3k/Reel